THAT WHICH IS CLAIMED IS:

1. An output buffer comprising:

supply voltage terminals;

an output stage including multiple, independently controllable output switches;

an output driver stage providing a control signal for the output stage; and

a correcting stage monitoring a supply voltage of at least one of the supply voltage terminals in view of the control signal, and dynamically controlling at least one of the controllable output switches so as to provide rapid response while limiting a supply voltage bounce at the supply voltage terminals within a predefined limit.

2. An output buffer according to Claim 1 wherein the correcting stage disables selected controllable output switches whenever a sensed supply voltage bounce increases beyond a predefined threshold level and enables selected controllable output switches whenever the sensed supply voltage bounce falls below the threshold voltage level.

3. An output buffer according to Claim 1 wherein the independently controllable output switches comprise switching transistors having output terminals connected together, and at least one of the switching transistors has a control terminal operated by the correcting stage.

4. An output buffer according to Claim 3 wherein the switching transistors comprise MOS transistors.

5. An output buffer according to Claim 4 wherein the MOS transistors are sized in a binary-weighted sequence.

6. An output buffer comprising:

supply voltage terminals;

an output stage including a plurality of independently controllable switching transistors having output terminals connected together;

an output driver stage providing a control signal for the output stage; and

a correcting stage monitoring a supply voltage of at least one of the supply voltage terminals, and controlling at least one of the controllable switching transistors to limit a supply voltage bounce at the supply voltage terminals within a predefined limit.

7. An output buffer according to Claim 6 wherein the correcting stage disables selected controllable switching transistors whenever a sensed supply voltage bounce increases beyond a predefined threshold level and enables selected controllable switching transistors whenever the sensed supply voltage bounce falls below the threshold voltage level.

8. An output buffer according to Claim 6 wherein at least one of the switching transistors has a control terminal operated by the correcting stage.

9. An output buffer according to Claim 8 wherein the switching transistors comprise MOS transistors.

10. An output buffer according to Claim 9 wherein the MOS transistors are sized in a binary-weighted sequence.

11. A method for reducing supply voltage bounce while maintaining speed of operation of an output buffer comprising:

providing multiple, independently controllable output switches in an output stage of the output buffer; and

monitoring a voltage of at least one supply terminal, with a correcting stage, whenever an input signal changes state and dynamically controlling at least one of the controllable output switches so as to provide rapid response while limiting a supply voltage bounce at the supply terminals within a predefined limit.

12. A method according to Claim 11 wherein the correcting stage disables selected controllable output switches whenever a sensed supply voltage bounce increases beyond a predefined threshold voltage level and enables selected controllable output switches whenever the sensed supply voltage bounce falls below the threshold voltage level.

13. A method for reducing supply voltage bounce while maintaining speed of operation of an output buffer comprising:

providing a plurality of independently controllable switching transistors having output terminals connected together in an output stage of the output buffer;

providing a control signal for the output stage; and

monitoring a voltage of at least one supply terminal, with a correcting stage, whenever the control signal changes state and dynamically controlling at least one of the controllable switching transistors to limit supply voltage bounce at the supply terminals within a predefined limit.

14. A method according to Claim 13 wherein the correcting stage disables selected controllable switching transistors whenever a sensed supply voltage bounce increases beyond a predefined threshold voltage level and enables selected controllable output switches whenever the sensed supply voltage bounce falls below the threshold voltage level.

15. A method according to Claim 14 wherein at least one of the switching transistors has a control terminal operated by the correcting stage.

16. A method according to Claim 14 wherein the switching transistors comprise MOS transistors.

17. A method according to Claim 16 wherein the MOS transistors are sized in a binary-weighted sequence.